In the Claims

Amend the claims as follows:

1. (currently amended) A method of detecting error during transfer of data signals from a data memory to a computer processor comprising:

commencing transmission of a raw data signal and an error detection code for the raw data signal from a data memory to a computer processor~~, the raw data signal including an error detection code~~;

at the time of the commencement of transmission of the raw data signal from the data memory to the computer processor, checking the raw data signal for corruption based on its error detection code;

if the data has not been corrupted, completing transmission of the raw data signal to the computer processor,

if the error detection code indicates data corruption, substituting the raw data signal with a predetermined reserved data signal and transmitting the predetermined reserved signal to the computer processor;

processing the data signal with the computer processor.

2. (currently amended) The method of claim 1 wherein, if the error detection code indicates data corruption, further including determining if the corrupted data in the ~~original~~ raw data signal may be corrected, and subsequently retrieving the corrected data and processing the corrected data signal with the computer processor.

3. (original) The method of claim 1 further including, if the computer processor processes the predetermined reserved signal, determining whether corrupted data in the raw data signal has been corrected, and, if corrected, retrieving the corrected data signal and processing the corrected data signal with the computer processor.

4. (original) The method of claim 1 further including, if the corrupted data in the raw data signal has been corrected, replacing the raw data signal in the data memory with the corrected raw data signal.

5. (original) The method of claim 1 further including, if the computer processor processes a predetermined reserved signal, the computer processor executes an error handling routine comprising determining whether corrupted data in the raw data signal has been corrected, and, if corrected, retrieving the corrected data signal, processing the corrected data signal with the computer processor, and replacing the raw data signal in the data memory with the corrected data signal.

6. (original) The method of claim 1 wherein the computer processor operates on timed, uniform clock cycles, and wherein the steps of transmitting the raw data signal from the data memory to a computer processor, simultaneously checking the raw data

signal for data corruption, and transmitting either the raw or predetermined reserved signal to the computer processor are performed within a clock cycle.

7. (original) The method of claim 1 further including commencing transmission of a subsequent raw data signal from the data memory to the computer processor and repeating the aforementioned steps for the subsequent raw data signal, until all desired raw data signals from the data memory are processed by the computer processor.

8. (original) The method of claim 1 wherein the raw data signal is a multi-bit data signal.

9. (original) The method of claim 1 wherein checking of the raw data signal for corruption by decoding the data and error detection code is performed simultaneously with the commencement of transmission of the raw data signal from the data memory to the computer processor.

10. (original) The method of claim 1 wherein the raw data signal is an instruction from a random access memory associated with the computer processor.

11. (currently amended) A system for detecting error during transfer of data signals from a data memory to a computer processor comprising:

a computer processor;

a data memory device containing raw data and an error detection code for the raw data to be processed by the computer processor, the raw data being in the form of a raw data signal ~~including an error detection code~~;

a data checker device adapted to check the raw data for corruption and, if the error detection code indicates data corruption, correcting the corrupted data in the raw data; and

a computer processor instruction unit, the instruction unit adapted to commence transmission of a raw data from the data memory device to the computer processor and cause the data checker device to check the raw data signal for corruption, the instruction unit further adapted to cause completion of transmission of the raw data to the computer processor if the error detection code indicates no data corruption or, if the error detection code indicates data corruption, cause substitution of the raw data with a predetermined reserved instruction and transmission of the predetermined reserved instruction to the computer processor.

12. (original) The system of claim 11 wherein the computer processor, upon processing a predetermined reserved instruction, is further adapted to execute an error handling routine comprising determining whether corrupted data in the raw data has been corrected, and, if corrected, retrieving the corrected data, processing the corrected data with the computer processor, and replacing the raw data in the data memory device with corrected data.

13. (original) The system of claim 11 wherein the computer processor includes a clock, the processor adapted to operate on timed, uniform clock cycles produced by the clock, and wherein the computer processor instruction unit is adapted to cause transmission of the raw data from the data memory device to the computer processor, the data checker device is adapted to check simultaneously the raw data for presence of corruption, and the computer processor instruction unit is adapted to transmit either the raw data or predetermined reserved instruction to the computer processor, within a clock cycle.

14. (original) The system of claim 11 further including a corrected data register adapted to receive data corrected by the data checker device and transmit corrected data to the computer processor.

15. (original) The system of claim 11 wherein the data memory device is a random access memory associated with the computer processor and the raw data is an instruction from the random access memory for the computer processor.

16. (currently amended) A program storage device readable by a machine, ~~tangibly~~ embodying a program of instructions executable by the machine to perform method steps for detecting error during transfer of a raw data ~~signals~~ signal and an error detection code for the raw data signal from a data memory to a computer processor, the raw data signal including an error detection code, the method comprising:

at the time of the commencement of transmission of the raw data signal from the data memory to the computer processor, checking the raw data signal for corruption;

if the error detection code indicates no data corruption, completing transmission of the raw data signal to the computer processor,

if the error detection code indicates data corruption, substituting the raw data signal with a predetermined reserved data signal and transmitting the predetermined reserved signal to the computer processor;

processing the data signal with the computer processor.

17. (currently amended) The program storage device of claim 16 wherein, if the error detection code indicates data corruption, the method further includes determining if the corrupted data in the ~~original~~ raw data signal may be corrected, and subsequently retrieving the corrected data and processing the corrected data signal with the computer processor.

18. (original) The program storage device of claim 16 wherein the method further includes, if the computer processor processes the predetermined reserved instruction, determining whether corrupted data in the raw data signal has been corrected, and, if corrected, retrieving the corrected data signal and processing the corrected data signal with the computer processor.

19. (original) The program storage device of claim 16 wherein the method further includes, if the corrupted data in the raw data signal has been corrected, replacing the raw data signal in the data memory with the corrected data signal.

20. (original) The program storage device of claim 16 wherein the error detection code comprises ECC code, and the raw data signal is an instruction from a random access memory associated with the computer processor.